Board Level Temperature Cycling Study of Large Array Wafer Level Package

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Abstract

The demand for Wafer Level Packages (WLP) has increased significantly due to its smaller package size and lower cost. However, board level reliability of WLP is still a major concern. This study investigates the board level temperature cycle reliability of three very different wafer level package configurations. Comprehensive studies are carried out through temperature cycle test, failure analysis, and finite element modeling. To assess the wafer level package capability and technology limit, the following parameters are considered: WLP structure, array size, ball locations, ball pitch, and temperature cycle profile.

Daisy-chain chips are used for this study. Extensive failure analysis was carried out to confirm failure mechanism and quantify the mechanical degradation among different solder joints due to temperature cycle stressing. It is suggested that the primary failure mechanism is solder fatigue. The crack is in bulk

printed circuit board (PCB) on the solder joint reliability of a WLCSP. Several studies were conducted to investigate

every daisy chain test chip. Failure rates for both groups are presented based on experimental data. This is the first time the effects of solder joint locations on the WLP reliability were verified experimentallyFatigue life as functions of array size and pitch is also presented. The effects of array size and ball pitch on the WLP reliability are also investigated.

Table 4. Normalized Characteristic Life for 0.5 mm and 0.4 mm Pitch WLP

Pitch	0.5 mm	0.4 mm
Characteristic Life	1	1.3

Temperature Cycle Profile:

A comparison of 1 cph and 2 cph temperature cycle rates is shown in Table 5. Again 12x12 array WLP-C structure is considered. It is observed that 2 cph has 20% longer fatigue life than 1 cph. Therefore, temperature profile has significant impact on failure rates. When comparing board level reliabilities among different WLP platforms, same temperature cycle conditions must be considered.

Table 5. Normalized Characteristic Life for 1cph and 2 cph

Temperature Cycle Rate	1 cph	2 cph
Characteristic Life (Normalized)	1	1.2

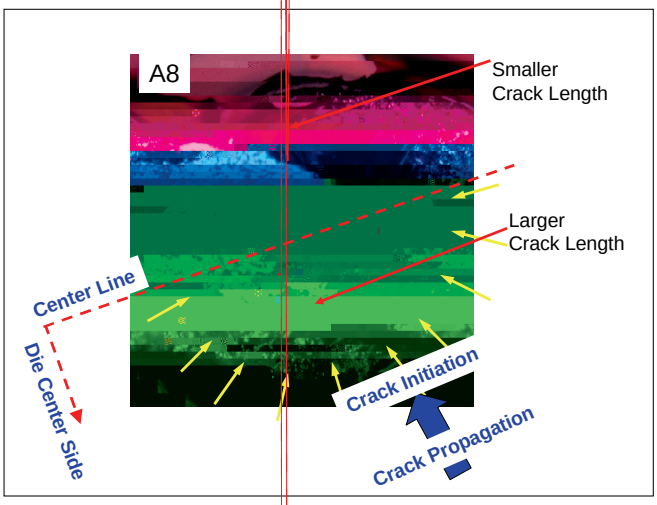

Figure 5. Crack Map of a Solder Ball (WLP B, Ball A8)

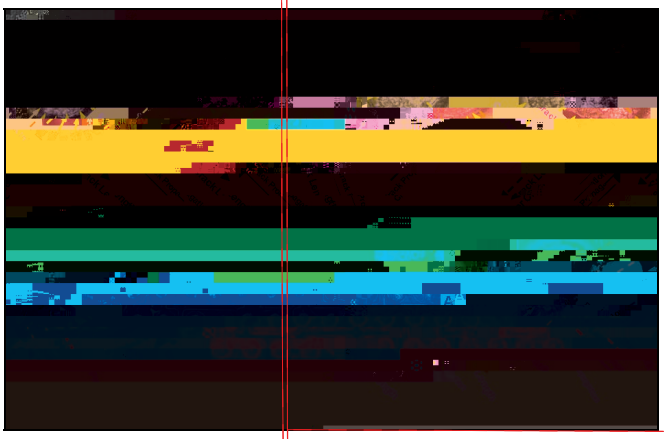

Figure 6. Crack Map and Propagation Direction of Solder
Balls (WLP B)

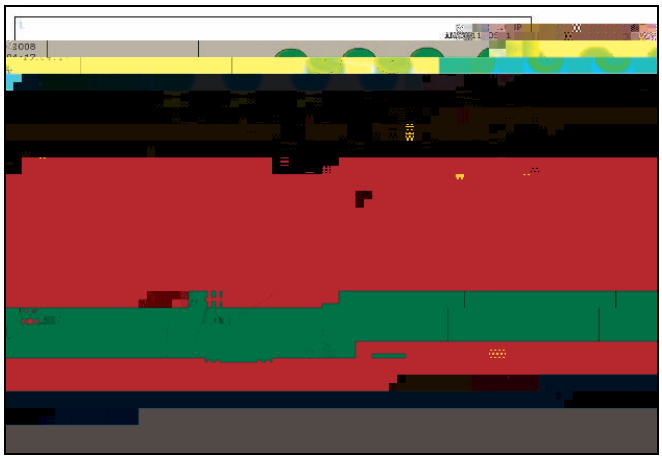

Figure 9. Von Mises Stress in Solder Balls for Identifying the Critical Ball

Summary and Conclusion

In this study, board level temperature cycle reliability of WLPs is studied through comprehensive tests, failure analysis and finite element modeling. The following conclusions can be made from this study:

1. WLP structure has great impact on solder joint reliability given that the same pitch and array size. Test results showed significantly different fatigue lives among the three WLP structures considered.
2. There is 20% fatigue life improvement from 12x12 array to 10x10 array size WLPs. And making corner balls not electrically connect